19-5182; Rev 1; 5/11

EVALUATION KIT AVAILABLE

1Gbps to 11.3Gbps, SFP+ Laser Driver with Laser Impedance Mismatch Tolerance

MAX3946

General Description

The MAX3946 is a +3.3V, multirate, low-power laser diode driver designed for Ethernet and Fibre Channel transmission systems at data rates up to 11.3Gbps. This device is optimized to drive a differential transmitter optical subassembly (TOSA) with a 25Ω flex circuit. The unique design of the output stage enables use of unmatched TOSAs, greatly reducing headroom limitations and lowering power consumption.

The device receives differential CML-compatible signals with on-chip line termination. It can deliver laser modulation current of up to 80mA, at an edge speed of 22ps (20% to 80%), into a 5Ω to 25Ω external differential load. The device is designed to have a symmetrical output stage with on-chip back terminations integrated into its outputs. A high-bandwidth, fully differential signal path is implemented to minimize deterministic jitter. An equalization block can be activated to compensate for the SFP+ connector. The integrated bias circuit provides programmable laser bias current up to 80mA. Both the laser bias generator and the laser modulator can be disabled from a single pin.

A 3-wire digital interface reduces the pin count and permits adjustment of input equalization, pulse-width adjustment, Tx polarity, Tx deemphasis, modulation current, and bias current without the need for external components. The MAX3946 is available in a 4mm x 4mm, 24-pin TQFN package.

Applications

4x/8x FC SFP+ Optical Transceivers

10GFC SFP+ Optical Transceivers

10GBASE-LR SFP+ Optical Transceivers

10GBASE-LRM SFP+ Optical Transceivers

OC192-SR XFP/SFP+ SDH/SONET Transceivers

Features

- ♦ **225mW Power Dissipation Enables < 1W SFP+ Modules**
- ♦ **Up to 100mW Power Consumption Reduction by Enabling the Use of Unmatched FP/DFB TOSAs**
- ♦ **Supports SFF-8431 SFP+ MSA and SFF-8472 Digital Diagnostic**
- ♦ **225mW Power Dissipation at 3.3V (I_{MOD} = 40mA, I_{BIAS} = 60mA Assuming 25Ω TOSA)**
- ♦ **Single +3.3V Power Supply**
- ♦ **Up to 11.3Gbps (NRZ) Operation**
- ♦ **Programmable Modulation Current from 10mA to 100mA (5Ω Load)**
- ♦ **Programmable Bias Current from 5mA to 80mA**
- ♦ **Programmable Input Equalization**
- ♦ **Programmable Output Deemphasis**
- ♦ **25Ω Output Back Termination at TOUT+ and TOUT-**
- ♦ **DJ Performance 7ps_{P-P} with Mismatched Differential Load (5Ω)**
- ♦ **DJ Performance 5ps_{P-P} with Mismatched Differential Load (25Ω)**
- ♦ **DJ Performance 5ps_{P-P} with 50Ω Differential Load**
- ♦ **Programmable Pulse Width**
- ♦ **Edge Transition Times of 22ps**
- ♦ **Bias Current Monitor**
- ♦ **Integrated Eye Safety Features**
- ♦ **3-Wire Digital Interface**
- ♦ **-40°C to +95°C Operation**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3946ETG+	-40°C to +85°C	24 TQFN-EP*

Note: *Parts are guaranteed by design and characterization to operate over the -40°C to +95°C ambient temperature range (T_A) and are tested up to +85°C.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

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ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{CCT}, V_{CCD} ....-0.3V to +4.0V
Current Into TOUT+ and TOUT-.................................... +100mA
Current Into TIN+ and TIN- .... -20mA to +20mA
Voltage Range at TIN+, TIN-,
DISABLE, SDA, SCL, CSEL, FAULT,
BMAX, and BMON................................ -0.3V to (V_{CC} + 0.3V)
Voltage Range at BIAS...-0.3V to V_{CC}
Voltage Range at TOUT+ and TOUT-....(V_{CC} - 1.3V) to (V_{CC} + 1.3V)
Current into BIAS...+130mA
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 27.8mW/°C above +70°C)..................2222mW
Storage Temperature Range ....-55°C to +150°C
Die Attach Temperature ....+400°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....36°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.63V, T_A = -40°C to +85°C, and Figure 1. Guaranteed by design and characterization from T_A = -40°C to +95°C. Typical values are at V_{CC} = +3.3V, I_{BIAS} = 60mA, I_{MOD} = 40mA, 25Ω differential output load, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Current	I_{CC}	Excludes output current through the external pullup inductors (Note 3)		68	90	mA
Power-Supply Voltage	V_{CC}		2.85		3.63	V
Power-Supply Noise		DC to 10MHz			100	mV_{P-P}
		10MHz to 20MHz			10	
POWER-ON RESET						
V_{CC} for Enable High				2.55	2.75	V
V_{CC} for Enable Low			2.3	2.45		V
DATA INPUT SPECIFICATION						
Input Data Rate			1	10	11.3	Gbps
Differential Input Voltage	V_{IN}	TXEQ_EN = high, launch amplitude into FR4 transmission line ≤ 5.5in	0.19		0.7	V_{P-P}
		TXEQ_EN = low	0.15		1.0	
Differential Input Resistance	R_{IN}		75	100	125	Ω
Differential Input Return Loss	SDD11	Part powered on, f ≤ 10GHz		12		dB
Common-Mode Input Return Loss	SCC11	Part powered on, 1GHz ≤ f ≤ 10GHz		10		dB
BIAS GENERATOR						
Maximum Bias Current	$I_{BIASMAX}$	Current into BIAS pin, DISABLE = low, and TX_EN = high	80			mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.85V to +3.63V, T_A = -40°C to +85°C, and Figure 1. Guaranteed by design and characterization from T_A = -40°C to +95°C. Typical values are at V_{CC} = +3.3V, I_{BIAS} = 60mA, I_{MOD} = 40mA, 25Ω differential output load, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Bias Current	$I_{BIASMIN}$	Current into BIAS pin, DISABLE = low, and TX_EN = high			5	mA
Bias-Off Current	$I_{BIAS-OFF}$	Current into BIAS pin, DISABLE = high or TX_EN = low or SET_IBIAS[8:0] = H0x00; BIAS pin voltage at V_{CC}			100	µA
Bias Current DAC Stability		5mA ≤ I_{BIAS} ≤ 80mA, V_{BIAS} = V_{CC} - 1.5V (Notes 2, 4)		1	3	%
Instantaneous Compliance Voltage at BIAS	V_{BIAS}		0.9	1.5	2.1	V
BMON Current Gain	G_{BMON}	G_{BMON} = I_{BMON}/I_{BIAS}, external resistor to ground defines voltage	9	10	11	mA/A
Compliance Voltage at BMON			0		1.8	V
BMON Current Gain Stability		5mA ≤ I_{BIAS} ≤ 80mA (Notes 2, 4)		1.2	4	%
LASER MODULATOR						
TOUT+ and TOUT- Instantaneous Output Compliance Voltage			V_{CC} - 1.0		V_{CC} + 1.0	V
Maximum Modulation Current	I_{MODMAX}	Current into external 25Ω differential termination, output common-mode voltage = V_{CC}	80			mA_{P-P}
		Current into external 50Ω differential termination, output common-mode voltage = V_{CC}	60			
Minimum Modulation Current	I_{MODMIN}				10	mA_{P-P}
Differential Output Resistance	2 x R_{OUT}			50		Ω
Modulation-Off Maximum Current	$I_{MOD-OFF}$	Current between TOUT+ and TOUT- when DISABLE = high or TX_EN = low or SET_IMOD[8:0] = H0x00			100	µA
Modulation Current DAC Stability		10mA ≤ I_{MOD} ≤ 80mA (Notes 2, 4)		1.5	3	%
Modulation Current Edge Speed (Note 2)	t_R, t_F	20% to 80%, 20mA ≤ I_{MOD} ≤ 80mA		22	30	ps
		20% to 80%, 10mA ≤ I_{MOD} ≤ 80mA, TXDE_MD[1:0] = 3d		22	30	
Deterministic Jitter (Notes 2, 5)	DJ	10mA ≤ I_{MOD} ≤ 60mA, 11.3Gbps, output differential load = 50Ω		5	12	ps_{P-P}
		10mA ≤ I_{MOD} ≤ 80mA, 11.3Gbps, output differential load = 25Ω		5	12	
		10mA ≤ I_{MOD} ≤ 80mA, 11.3Gbps, output differential load = 5Ω		7		
		10mA ≤ I_{MOD} ≤ 60mA, 10.7Gbps, output differential load = 50Ω (K28.5 pattern)		5	10.5	

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.85V to +3.63V, T_A = -40°C to +85°C, and Figure 1. Guaranteed by design and characterization from T_A = -40°C to +95°C. Typical values are at V_{CC} = +3.3V, I_{BIAS} = 60mA, I_{MOD} = 40mA, 25Ω differential output load, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Random Jitter	RJ	10mA ≤ I_{MOD} ≤ 80mA, output differential load = 25Ω (Note 2)		0.19	0.55	ps_{RMS}
Differential Output Return Loss	SDD22	Part powered on, f ≤ 5GHz		8		dB
		Part powered on, f ≤ 10GHz		6		
SAFETY FEATURES						
Threshold Voltage at BMAX	V_{BMAX}	FAULT always occurs for V_{BMAX} ≥ 1.3V, FAULT never occurs for V_{BMAX} < 1.1V (Note 2, Figure 1)	1.1	1.2	1.3	V
Threshold Voltage at BIAS	V_{BIAS}	FAULT never occurs for V_{BIAS} ≥ 0.57V, FAULT always occurs for V_{BIAS} < 0.44V	0.44	0.48	0.57	V
Threshold Voltage at BMON	V_{BMON}	Warning always occurs for V_{BMON} ≥ V_{CC} - 0.5V, warning never occurs for V_{BMON} < V_{CC} - 0.7V	V_{CC} - 0.7	V_{CC} - 0.6	V_{CC} - 0.5	V
SFP TIMING REQUIREMENTS						
DISABLE Assert Time	t_OFF	Time from rising edge of DISABLE input signal to I_{BIAS} < $I_{BIAS-OFF}$ and I_{MOD} < $I_{MOD-OFF}$		0.05	1	µs
DISABLE Negate Time	t_ON	Time from falling edge of DISABLE to I_{BIAS} and I_{MOD} at 90% of steady state		0.5	5	µs
FAULT Reset Time of Power-On Time	t_INIT	Time from power-on or negation of FAULT using DISABLE		50	200	µs
FAULT Reset Time	t_FAULT	Time from fault to FAULT on, C_{FAULT} ≤ 20pF, R_{FAULT} = 4.7kΩ		0.5	2	µs
DISABLE to Reset		Time DISABLE must be held high to reset FAULT	0.5			µs
BIAS CURRENT DAC						
Full-Scale Current	$I_{BIAS-FS}$	SET_IBIAS[8:1] = HxFF	80	100		mA
LSB Size				190		µA
Integral Nonlinearity	INL	5mA ≤ I_{BIAS} ≤ 80mA		±0.5		%FS
Differential Nonlinearity	DNL	5mA ≤ I_{BIAS} ≤ 80mA, guaranteed monotonic at 8-bit resolution SET_IBIAS[8:1]		±0.5		LSB
MODULATION CURRENT DAC (25Ω DIFFERENTIAL LOAD)						
Full-Scale Current	I_{MOD-FS}	SET_IMOD[8:1] = HxFF	80	105		mA
LSB Size				200		µA
Integral Nonlinearity	INL	10mA ≤ I_{MOD} ≤ 80mA		±1		%FS
Differential Nonlinearity	DNL	10mA ≤ I_{MOD} ≤ 80mA, guaranteed monotonic at 9-bit resolution SET_IMOD[8:0]		±0.5		LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.85V to +3.63V, T_A = -40°C to +85°C, and Figure 1. Guaranteed by design and characterization from T_A = -40°C to +95°C. Typical values are at V_{CC} = +3.3V, I_{BIAS} = 60mA, I_{MOD} = 40mA, 25Ω differential output load, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL I/O SPECIFICATIONS						
DISABLE Input Current	I_{IH}				12	µA
	I_{IL}	Depends on pullup resistance		500	800	
DISABLE Input High Voltage	V_{IH}		1.8		V_{CC}	V
DISABLE Input Low Voltage	V_{IL}		0		0.8	V
DISABLE Input Resistance	R_{PULL}	Internal pullup resistor	4.7	7.5	10	kΩ
3-WIRE DIGITAL I/O SPECIFICATIONS (SDA, SCL, CSEL)						
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYST}			80		mV
Input Leakage Current	I_{IL}, I_{IH}	V_{IN} = 0V or V_{CC}, internal pullup or pulldown is 75kΩ typical			150	µA
Output High Voltage	V_{OH}	External pullup is (4.7kΩ to 10kΩ) to V_{CC}	V_{CC} - 0.5			V
Output Low Voltage	V_{OL}	External pullup is (4.7kΩ to 10kΩ) to V_{CC}			0.4	V
3-WIRE DIGITAL INTERFACE TIMING CHARACTERISTICS (Figure 5)						
SCL Clock Frequency	f_{SCL}			400	1000	kHz
SCL Pulse-Width High	t_{CH}		0.5			µs
SCL Pulse-Width Low	t_{CL}		0.5			µs
SDA Setup Time	t_{DS}			100		ns
SDA Hold Time	t_{DH}			100		ns
SCL Rise to SDA Propagation Time	t_D			5		ns
CSEL Pulse-Width Low	t_{CSW}		500			ns
CSEL Leading Time Before the First SCL Edge	t_L			500		ns
CSEL Trailing Time After the Last SCL Edge	t_T			500		ns
SDA, SCL Load	C_B	Total bus capacitance on one line with 4.7kΩ pullup to V_{CC}			20	pF

Note 2: Guaranteed by design and characterization (T_A = -40°C to +95°C).

Note 3: BIAS is connected to 2.0V. TOUT+/TOUT- are connected through pullup inductors to a separate supply that is equal to V_{CCT}.

Note 4: Stability is defined as [(I_measured) - (I_reference)]/(I_reference) over the listed current range, temperature, and V_{CC} = V_{CCREF} ±5%. V_{CCREF} = 3.0V to 3.45V. Reference current measured at V_{CCREF}, T_A = +25°C.

Note 5: Measured with K28.5 data pattern at 10.7Gbps and with a (2^7 - 1 PRBS + 72 zeros + 2^7 - 1 PRBS (inverted) + 72 ones) pattern at 11.3Gbps.

1Gbps to 11.3Gbps, SFP+ Laser Driver with Laser Impedance Mismatch Tolerance

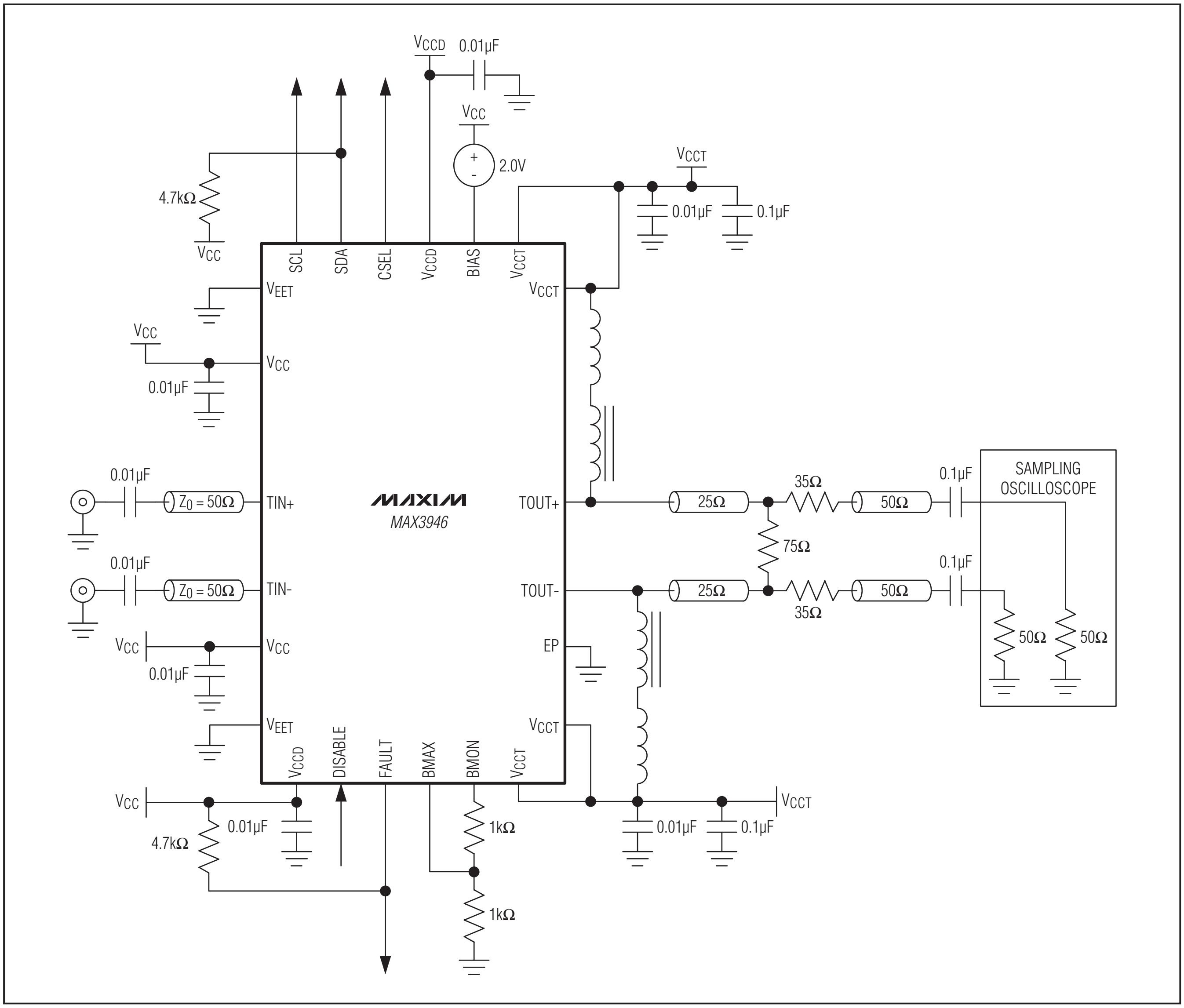
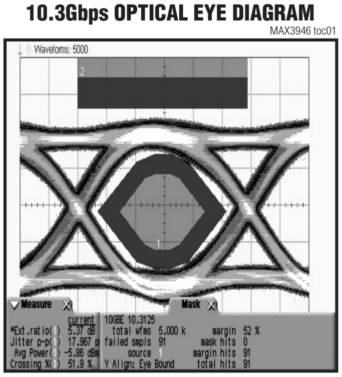


Figure 1. AC Test Setup

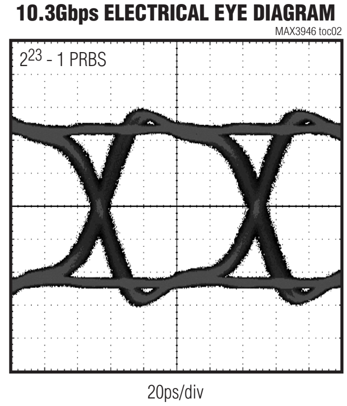
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^7 - 1 PRBS + 72 zeros + 2^7 - 1 PRBS (inverted) +72 ones, unless otherwise noted.)

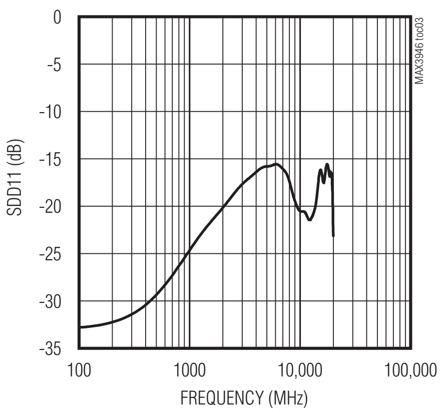
10.3Gbps OPTICAL EYE DIAGRAM



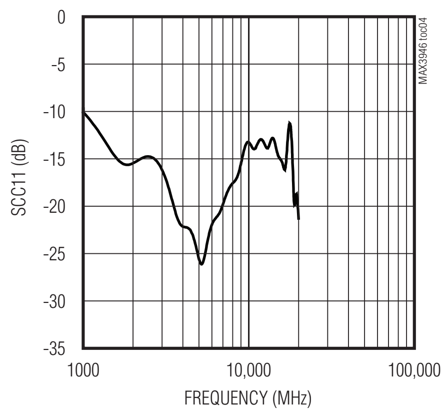
10.3Gbps ELECTRICAL EYE DIAGRAM



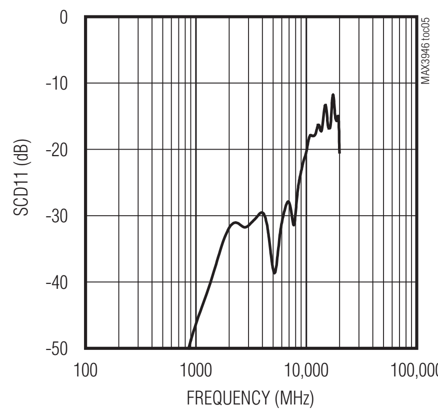
INPUT DIFFERENTIAL RETURN LOSS vs. FREQUENCY



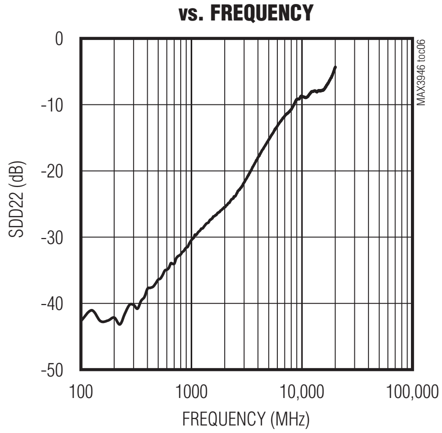
INPUT COMMON-MODE RETURN LOSS vs. FREQUENCY



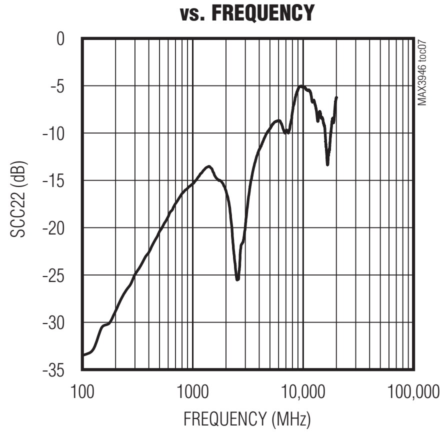
INPUT DIFFERENTIAL TO COMMON-MODE RETURN LOSS vs. FREQUENCY



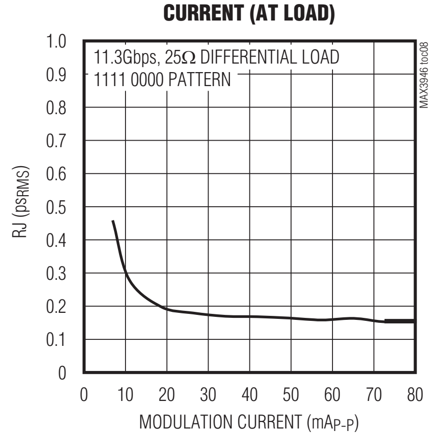
OUTPUT DIFFERENTIAL RETURN LOSS vs. FREQUENCY



OUTPUT COMMON-MODE RETURN LOSS vs. FREQUENCY



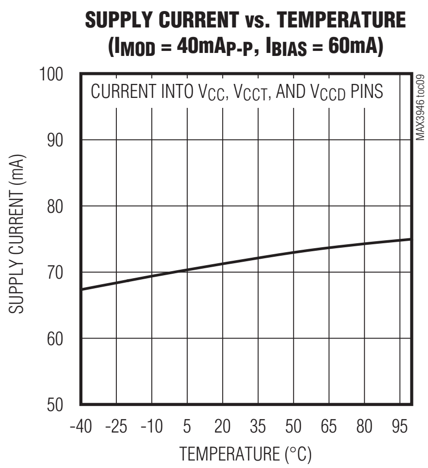
RANDOM JITTER vs. MODULATION CURRENT (AT LOAD)

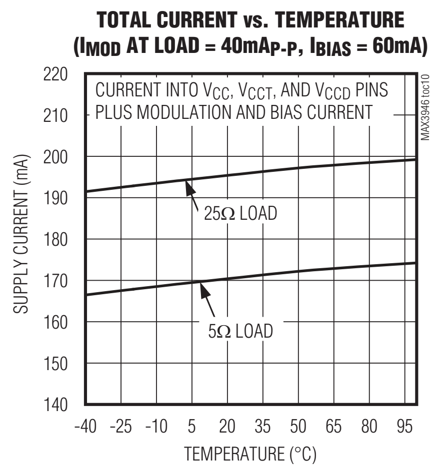


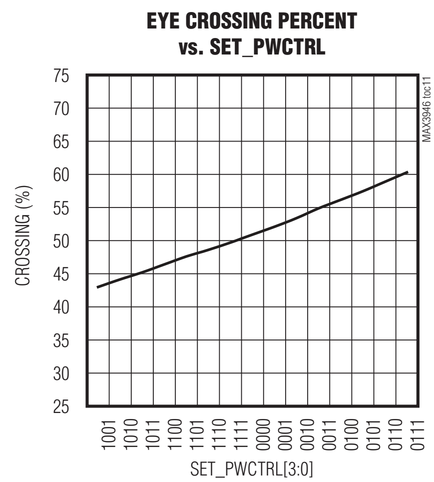
1Gbps to 11.3Gbps, SFP+ Laser Driver with Laser Impedance Mismatch Tolerance

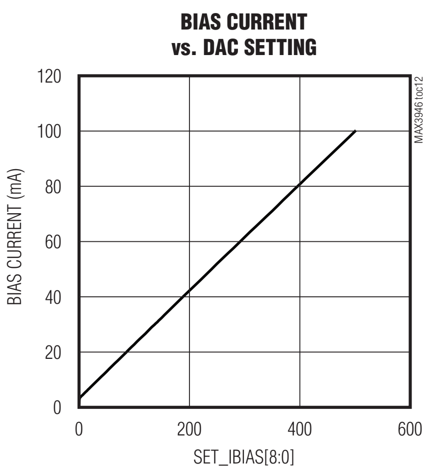
Typical Operating Characteristics (continued)

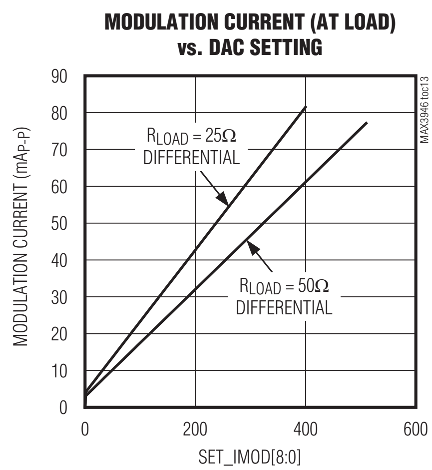
(V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^7 - 1 PRBS + 72 zeros + 2^7 - 1 PRBS (inverted) +72 ones, unless otherwise noted.)

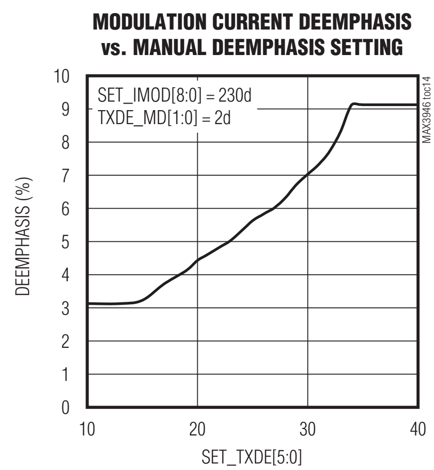


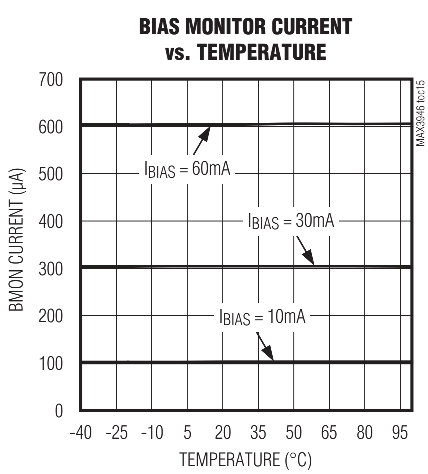


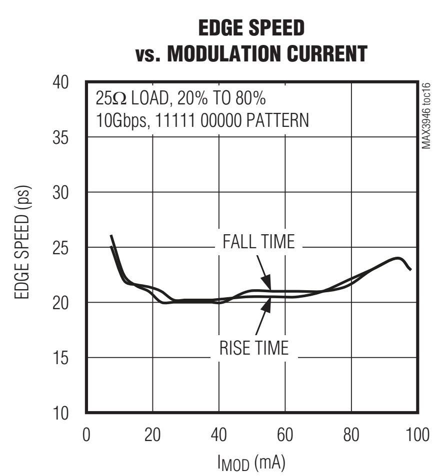


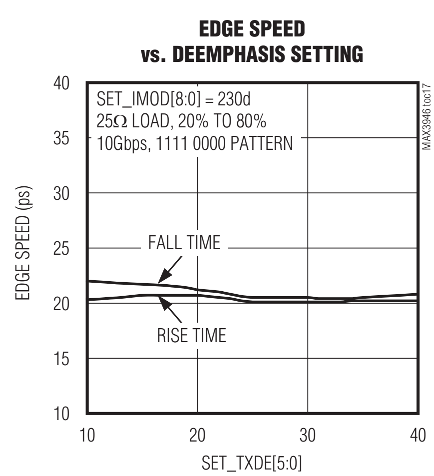












Typical Operating Characteristics (continued)

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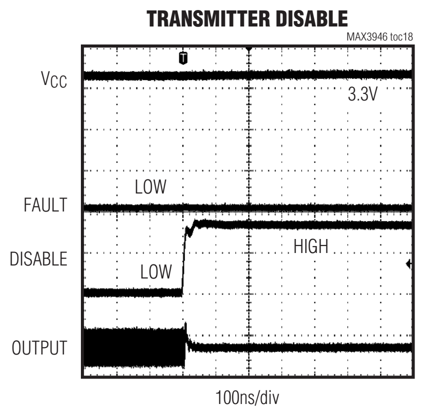

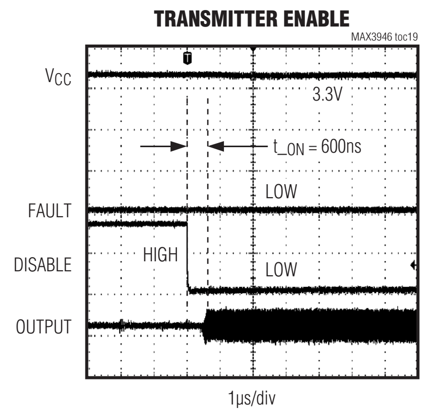

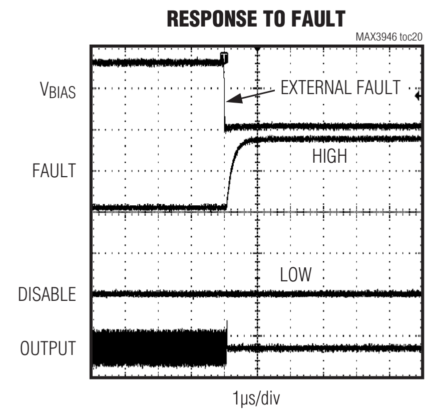

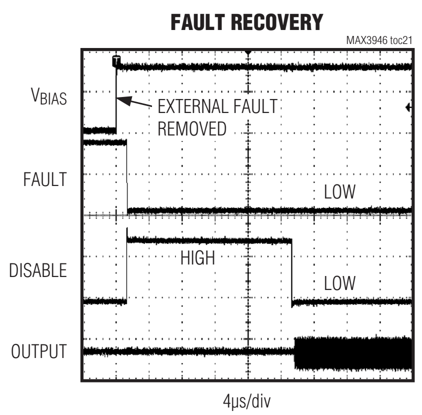

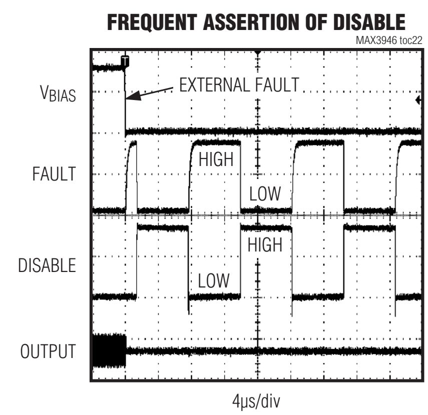

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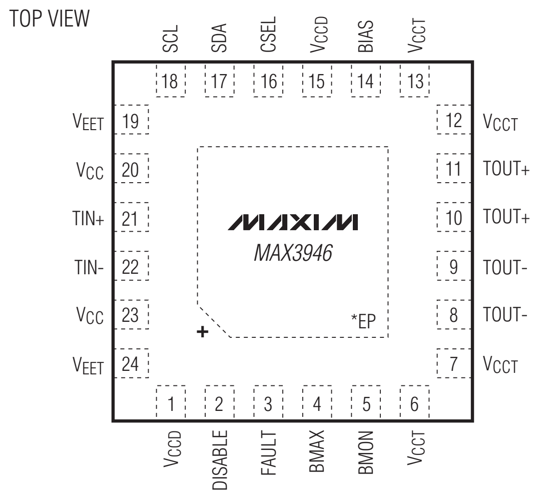
Pin Configuration



THIN QFN
(4mm × 4mm)

*EXPOSED PAD CONNECTED TO GROUND.

Pin Description

PIN	NAME	FUNCTION
1, 15	V_{CCD}	Power Supply. Provides supply voltage to the digital block.
2	DISABLE	Disable Input, CMOS. Set to logic-low for normal operation. Logic-high or open disables both the modulation current and the bias current. Internally pulled up by a 7.5kΩ resistor to V_{CCD}.
3	FAULT	Fault Output, Open Drain. Logic-high indicates a fault condition. FAULT remains high even after the fault condition has been removed. A logic-low occurs when the fault condition has been removed and the fault latch has been cleared by toggling the DISABLE pin. FAULT should be pulled up to V_{CC} by a 4.7kΩ to 10kΩ resistor.
4	BMAX	Analog Laser Bias-Current Limit. A resistive voltage-divider connected among BMON, BMAX, and ground sets the maximum allowed laser bias current limit. The voltage at BMAX is internally compared to 1.2V bandgap reference voltage.
5	BMON	Bias Current-Monitor Output. Current out of this pin develops a ground-referenced voltage across external resistor(s) that is proportional to the laser bias current. The current sourced by this pin is typically 1/100th the BIAS pin current.
6, 7, 12, 13	V_{CCT}	Power Supply. Provides supply voltage to the output block.
8, 9	TOUT-	Inverted Modulation Current Output. Internally pulled up by a 25Ω resistor to V_{CCT}.
10, 11	TOUT+	Noninverted Modulation Current Output. Internally pulled up by a 25Ω resistor to V_{CCT}.
14	BIAS	Laser Bias Current Connection. This pin requires a 0.1µF capacitor to V_{EET} for proper operation.
16	CSEL	Chip-Select Input, CMOS. Setting CSEL to logic-high starts a cycle. Setting CSEL to logic-low ends the cycle and resets the control state machine. Internally pulled down by a 75kΩ resistor to V_{EET}.
17	SDA	Serial-Data Bidirectional Input, CMOS. Open-drain output. This pin has a 75kΩ internal pullup, but it requires an external 4.7kΩ to 10kΩ pullup resistor. (Data line-collision protection is implemented.)

Pin Description (continued)

PIN	NAME	FUNCTION
18	SCL	Serial-Clock Input, CMOS. This pin has a 75kΩ internal pulldown.
19, 24	V_{EET}	Ground
20, 23	V_{CC}	Power-Supply Connections. Provides supply voltage to the core circuitry.
21	TIN+	Noninverted Data Input
22	TIN-	Inverted Data Input
—	EP	Exposed Pad. Ground. Must be soldered to circuit board ground for proper thermal and electrical performance (see the *Exposed-Pad Package and Thermal Considerations* section).

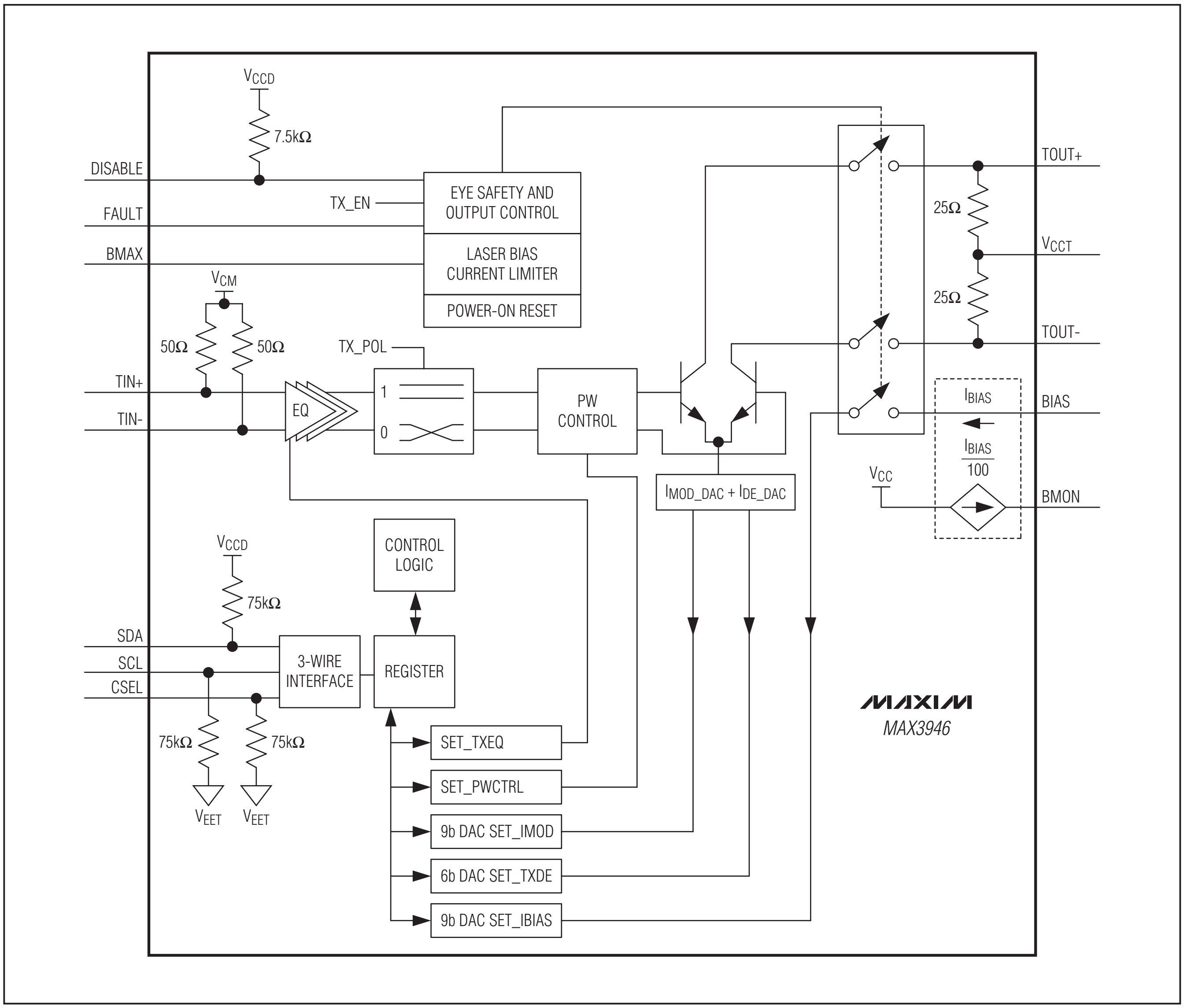


Figure 2. Functional Diagram

1Gbps to 11.3Gbps, SFP+ Laser Driver with Laser Impedance Mismatch Tolerance

Detailed Description

The MAX3946 SFP+ laser driver is designed to drive 5Ω to 50Ω TOSAs from 1Gbps to 11.3Gbps. The device contains an input buffer with programmable equalization, pulse-width adjustment, bias current and modulation current DACs, output driver with programmable deemphasis, power-on reset circuitry, bias monitor, laser current limiter, and eye-safety circuitry. A 3-wire digital interface is used to control the transmitter functions. The registers that control the device's functionality are TXCTRL, SET_IMOD, SET_IBIAS, IMODMAX, IBIASMAX, MODINC, BIASINC, SET_TXEQ, SET_PWCTRL, and SET_TXDE.

Input Buffer with Programmable Equalization

The input is internally biased and terminated with 50Ω to a common-mode voltage. The first amplifier stage features a programmable equalizer for high-frequency losses including SFP connector. Equalization is controlled by the SET_TXEQ register and TXEQ_EN bit, TXCTRL[3] (Table 1). The TX_POL bit in the TXCTRL register controls the polarity of TOUT+ and TOUT- vs. TIN+ and TIN-. The SET_PWCTRL register controls the output eye crossing (Table 5). A status indicator bit (TXED) monitors the presence of an AC input signal.

Bias Current DAC

The device's bias current is optimized to provide up to 80mA of bias current into a 5Ω to 50Ω laser load with 200µA resolution. The bias current is controlled through the 3-wire digital interface using the SET_IBIAS, IBIASMAX, and BIASINC registers.

For laser operation, the laser bias current can be set using the 9-bit SET_IBIAS DAC. The upper 8 bits are set by the SET_IBIAS[8:1] register, commonly used during the initialization procedure after POR. The LSB (bit 0) of SET_IBIAS is initialized to zero after POR and can be updated using the BIASINC register. The IBIASMAX register should be programmed to a desired maximum bias current value (up to 96mA) to protect the laser. The IBIASMAX register limits the maximum SET_IBIAS[8:1] DAC code.

After initialization the value of the SET_IBIAS DAC register should be updated using the BIASINC register to optimize cycle time and enhance laser safety. The BIASINC register is an 8-bit register where the first 5 bits contain the increment information in two's complement notation. Increment values range from -16 to +15 LSBs. If the updated value of SET_IBIAS[8:1] exceeds IBIASMAX[7:0], the IBIASERR warning flag is set and SET_IBIAS[8:0] remains unchanged.

Modulation Current DAC

The modulation current from the device is optimized to provide up to 80mA of modulation current into a 5Ω to 25Ω differential laser load (60mA for 50Ω laser load) with 300µA to 200µA resolution. The modulation current is controlled through the 3-wire digital interface using the SET_IMOD, IMODMAX, MODINC, and SET_TXDE registers.

For laser operation, the laser modulation current can be set using the 9-bit SET_IMOD DAC. The upper 8 bits are set by the SET_IMOD[8:1] register, commonly used during the initialization procedure after POR. The LSB (bit 0) of SET_IMOD is initialized to zero after POR and can be updated using the MODINC register. The IMODMAX register should be programmed to a desired maximum modulation current value (up to 96mA) to protect the laser. The IMODMAX register limits the maximum SET_IMOD[8:1] DAC code.

Table 1. Input Equalization Control Register Settings

TXCTRL[3] TXEQ_EN	SET_TXEQ[2:1]		DESCRIPTION
0	X	X	150mV$_{P-P}$ to 1000mV$_{P-P}$ differential input amplitude (default setting)
1	0	0	Optimized for 1in to 4in FR4, 190mV$_{P-P}$ to 450mV$_{P-P}$ differential launch amplitude from source
1	0	1	Optimized for 4in to 6in FR4, 190mV$_{P-P}$ to 450mV$_{P-P}$ differential launch amplitude from source
1	1	0	Optimized for 1in to 4in FR4, 450mV$_{P-P}$ to 700mV$_{P-P}$ differential launch amplitude from source
1	1	1	Optimized for 4in to 6in FR4, 450mV$_{P-P}$ to 700mV$_{P-P}$ differential launch amplitude from source

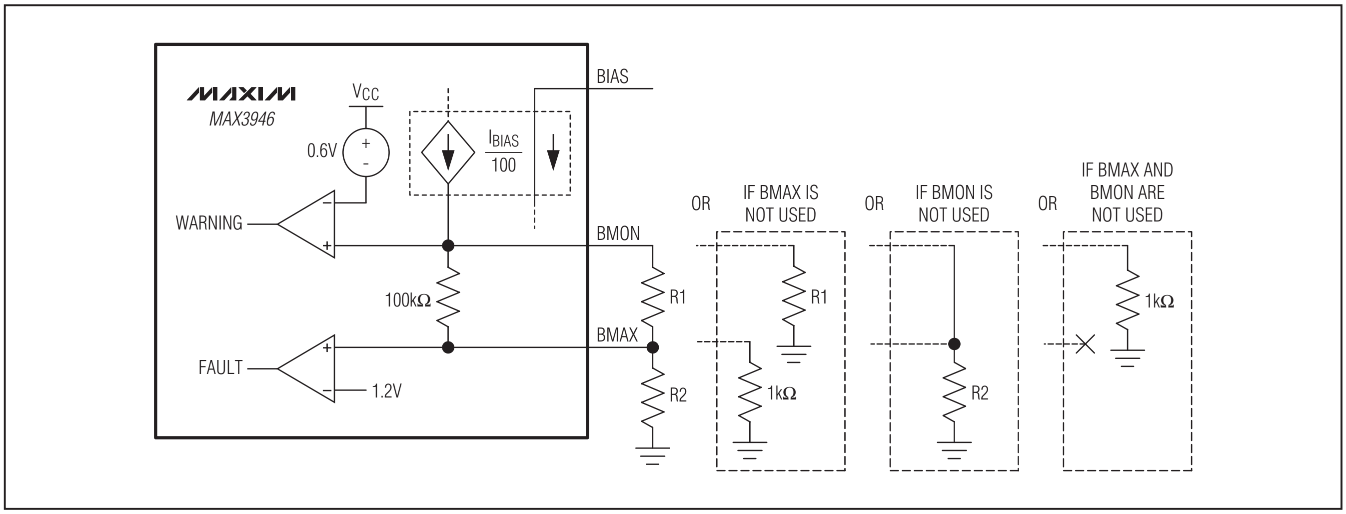


Figure 3. BMON and BMAX Circuitry

After initialization the value of the SET_IMOD DAC register should be updated using the MODINC register to optimize cycle time and enhance laser safety. The MODINC register is an 8-bit register where the first 5 bits contain the increment information in two's complement notation. Increment values range from -16 to +15 LSBs. If the updated value of SET_IMOD[8:1] exceeds IMODMAX[7:0], the IMODERR warning flag is set and SET_IMOD[8:0] remains unchanged.

Modulation current sent to the laser is actually the combination of the current generated by the SET_IMOD register and current subtracted from this by the SET_TXDE register.

Output Driver

The output driver is optimized for a 5Ω to 50Ω differential load. The output stage also features programmable deemphasis that can be set as a percentage of the modulation current. The deemphasis function is controlled by the TXDE_MD[1] and TXDE_MD[0] bits (TXCTRL[5:4]) and SET_TXDE[5:0].

Power-On Reset (POR)

POR ensures that the laser is off until supply voltage has reached a specified threshold (2.75V). After POR, bias current and modulation current ramps are controlled to avoid overshoot. In the case of a POR, all registers are reset to their default values.

BMON and BMAX Functions

Current out of the BMON pin is typically 1/100th the value of the current at the BIAS pin. The total resistance to ground at BMON sets the voltage gain. An internal comparator at the BMAX pin latches a fault if the voltage on BMAX exceeds the value of 1.2V. The BMAX voltage-sense pin is connected by means of a voltage-divider to the BMON pin and ground. The full-scale range of the BMON voltage is 1.2V x (R1/R2 + 1) (Figure 3). The analog bias-current limit is determined by (1.2V/R2) x 100.

Eye Safety and Output Control Circuitry

The safety and output control circuitry includes the disable pin (DISABLE) and disable bit (TX_EN), along with a fault indicator and fault detectors (Figure 4). The device has two types of faults, HARD FAULT and SOFT FAULT. A HARD FAULT triggers the FAULT pin, and the output to the laser is disabled. A SOFT FAULT operates as a warning, and the outputs are not disabled. Both types of faults are stored in the TXSTAT1 and TXSTAT2 registers.

The FAULT pin is a latched output that can be cleared by toggling the DISABLE pin. Toggling the DISABLE pin also clears the TXSTAT1 and TXSTAT2 registers. A single-point fault can be a short to V_{CC} or ground. Table 2 shows the circuit response to various single-point faults.

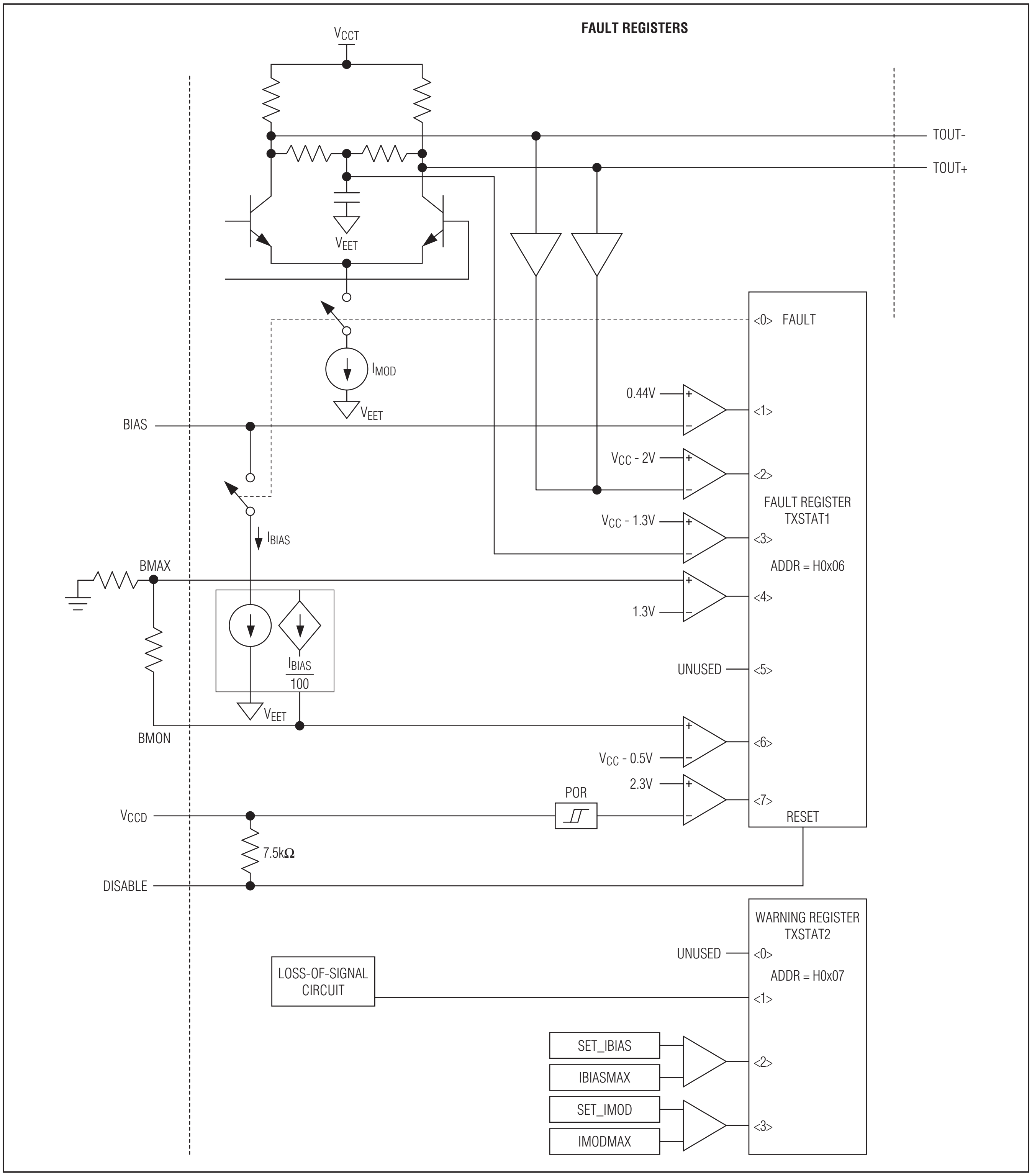


Figure 4. Eye Safety Circuitry

Table 2. Circuit Response to Single-Point Faults

PIN	NAME	SHORT TO V_{CC}	SHORT TO GROUND	OPEN
1	V_{CCD}	Normal	Disabled—HARD FAULT	Normal (Note 3)—Redundant path
2	DISABLE	Disabled	Normal (Note 1). Can only be disabled by other means.	Disabled
3	FAULT	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
4	BMAX	Disabled—HARD FAULT	Normal (Note 1)	Disabled—HARD FAULT
5	BMON	Disabled—HARD FAULT	Normal (Note 1)	Disabled—HARD FAULT
6	V_{CCT}	Normal	Disabled—Fault (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
7	V_{CCT}	Normal	Disabled—Fault (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
8	TOUT-	I_{MOD} is reduced	Disabled—HARD FAULT	I_{MOD} is reduced
9	TOUT-	I_{MOD} is reduced	Disabled—HARD FAULT	I_{MOD} is reduced
10	TOUT+	I_{MOD} is reduced	Disabled—HARD FAULT	I_{MOD} is reduced
11	TOUT+	I_{MOD} is reduced	Disabled—HARD FAULT	I_{MOD} is reduced
12	V_{CCT}	Normal	Disabled—Fault (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
13	V_{CCT}	Normal	Disabled—Fault (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
14	BIAS	I_{BIAS} is on—No fault	Disabled—HARD FAULT	Disabled—HARD FAULT
15	V_{CCD}	Normal	Disabled—Fault (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
16	CSEL	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
17	SDA	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
18	SCL	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
19	V_{EET}	Disabled—Fault (external supply shorted) (Note 2)	Normal	Normal (Note 3)—Redundant path
20	V_{CC}	Normal	Disabled—HARD FAULT (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
21	TIN+	SOFT FAULT	SOFT FAULT	Normal (Note 1)
22	TIN-	SOFT FAULT	SOFT FAULT	Normal (Note 1)
23	V_{CC}	Normal	Disabled—HARD FAULT (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
24	V_{EET}	Disabled—Fault (external supply shorted) (Note 2)	Normal	Normal (Note 3)—Redundant path

Note 1: Normal—Does not affect laser power.
Note 2: Supply-shorted current is assumed to be primarily on the circuit board (outside this device), and the main supply is collapsed by the short.
Note 3: Normal in functionality, but performance could be affected.
Warning: Shorted to V_{CC} or shorted to ground on some pins can violate the *Absolute Maximum Ratings*.

1Gbps to 11.3Gbps, SFP+ Laser Driver with Laser Impedance Mismatch Tolerance

3-Wire Interface

The device implements a proprietary 3-wire digital interface. An external controller generates the clock. The 3-wire interface consists of an SDA bidirectional data line, an SCL clock signal input, and a CSEL chip-select input (active high). The external master initiates a data transfer by asserting the CSEL pin. The master starts to generate a clock signal after the CSEL pin has been set to a logic-high. All data transfers are most significant bit (MSB) first.

Protocol

Each operation consists of 16-bit transfers (15-bit address/data, 1-bit RWN). The bus master generates 16 clock cycles to SCL. All operations transfer 8 bits to the device. The RWN bit determines if the cycle is read or write. See Table 3.

Register Addresses

The device contains 13 registers available for programming. Table 4 shows the registers and addresses.

Write Mode (RWN = 0)

The master generates 16 total clock cycles at SCL. The master outputs a total of 16 bits (MSB first) to the SDA line at the falling edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 5 shows the interface timing.

Read Mode (RWN = 1)

The master generates 16 total clock cycles at SCL. The master outputs a total of 8 bits (MSB first) to the SDA line at the falling edge of the clock. The SDA line is released after the RWN bit has been transmitted. The slave outputs 8 bits of data (MSB first) at the rising edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 5 shows the interface timing.

Mode Control

Normal mode allows read-only instruction for all registers except MODINC and BIASINC. The MODINC and BIASINC registers can be updated during normal mode. Doing so speeds up the laser control update through the 3-wire interface by a factor of two. The normal mode is the default mode.

Setup mode allows the master to write unrestricted data into any register except the status (TXSTAT1, TXSTAT2) registers. To enter the setup mode, the MODECTRL register (address = H0x0E) must be set to H0x12. After the MODECTRL register has been set to H0x12, the next operation is unrestricted. The setup mode is automatically exited after the next operation is finished. This sequence must be repeated if further unrestricted settings are necessary.

Table 3. Digital Communication Word Structure

BIT															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Register Address							RWN	Data that is written or read							

Table 4. Register Descriptions and Addresses

ADDRESS	NAME	FUNCTION
H0x05	TXCTRL	Transmitter Control Register
H0x06	TXSTAT1	Transmitter Status Register 1
H0x07	TXSTAT2	Transmitter Status Register 2
H0x08	SET_IBIAS	Bias Current Setting Register
H0x09	SET_IMOD	Modulation Current Setting Register
H0x0A	IMODMAX	Maximum Modulation Current Setting Register
H0x0B	IBIASMAX	Maximum Bias Current Setting Register
H0x0C	MODINC	Modulation Current Increment Setting Register
H0x0D	BIASINC	Bias Current Increment Setting Register
H0x0E	MODECTRL	Mode Control Register
H0x0F	SET_PWCTRL	Pulse-Width Control Register
H0x10	SET_TXDE	Deemphasis Control Register
H0x11	SET_TXEQ	Equalization Control Register

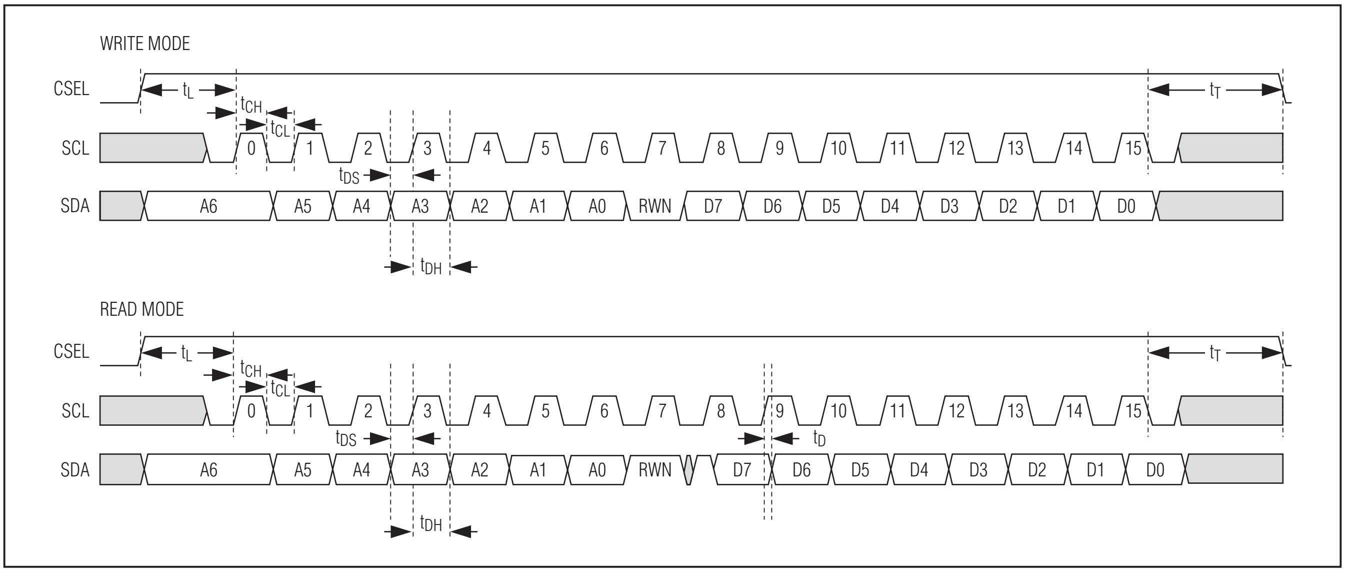


Figure 5. Timing for 3-Wire Digital Interface

Transmitter Control Register (TXCTRL)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	X	TXDE_MD[1]	TXDE_MD[0]	TXEQ_EN	SOFTRES	TX_POL	TX_EN	H0x05
Default Value	X	X	0	0	0	0	1	1	

Bits 5 and 4: TXDE_MD[1:0]. Controls the mode of the transmit output deemphasis circuitry.

00 = deemphasis is fixed at 6.25% of the modulation amplitude

01 = deemphasis is fixed at 3.125% of the modulation amplitude

10 = deemphasis is programmed by the SET_TXDE register setting

11 = deemphasis is at its maximum of approximately 9%

Bit 3: TXEQ_EN. Enables or disables the input equalization circuitry.

0 = disabled

1 = enabled

Bit 2: SOFTRES. Resets all registers to their default values (the DISABLE pin must be at a logic 1 during a write to SOFTRES for the registers to be set to their default values).

0 = normal

1 = reset

Bit 1: TX_POL. Controls the polarity of the signal path.

0 = inverse

1 = normal

Bit 0: TX_EN. Enables or disables the output circuitry.

0 = disabled

1 = enabled

Transmitter Status Register 1 (TXSTAT1)

Bit #	7 (STICKY)	6 (STICKY)	5 (STICKY)	4 (STICKY)	3 (STICKY)	2 (STICKY)	1 (STICKY)	0 (STICKY)	ADDRESS
Name	FST[7]	FST[6]	X	FST[4]	FST[3]	FST[2]	FST[1]	TX_FAULT	H0x06
Default Value	X	X	X	X	X	X	X	X	

Bit 7: FST[7]. When the V_{CCT} supply voltage is below 2.3V, the POR circuitry reports a fault. Once the V_{CCT} supply voltage is above 2.75V, the POR resets all registers to their default values and the fault is cleared.

Bit 6: FST[6]. When the voltage at BMON is above V_{CC} - 0.5V, a SOFT FAULT is reported.

Bit 4: FST[4]. When the voltage at BMAX goes above 1.3V, a HARD FAULT is reported.

Bit 3: FST[3]. When the common-mode voltage at $V_{TOUT\pm}$ goes below V_{CC} - 1.3V, a SOFT FAULT is reported.

Bit 2: FST[2]. When the voltage at $V_{TOUT\pm}$ goes below V_{CC} - 0.8V, a HARD FAULT is reported.

Bit 1: FST[1]. When the BIAS voltage goes below 0.44V, a HARD FAULT is reported.

Bit 0: TX_FAULT. Copy of a FAULT signal in FST[7:6] and FST[4:1]. A POR resets the FST bits to 0.

Transmitter Status Register 2 (TXSTAT2)

Bit #	7	6	5	4	3 (STICKY)	2 (STICKY)	1 (STICKY)	0 (STICKY)	ADDRESS
Name	X	X	X	X	IMODERR	IBIASERR	TXED	X	H0x07
Default Value	X	X	X	X	X	X	X	X	

Bit 3: IMODERR. Any attempt to modify SET_IMOD[8:1] above IMODMAX[7:0] flags a warning at IMODERR. (See the *Programming Modulation Current* section.)

Bit 2: IBIASERR. Any attempt to modify SET_IBIAS[8:1] above IBIASMAX[7:0] flags a warning at IBIASERR. (See the *Programming Bias Current* section.)

Bit 1: TXED. This indicates the absence of an AC signal at the transmit input.

Bias Current Setting Register (SET_IBIAS)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	SET_IBIAS [8] (MSB)	SET_IBIAS [7]	SET_IBIAS [6]	SET_IBIAS [5]	SET_IBIAS [4]	SET_IBIAS [3]	SET_IBIAS [2]	SET_IBIAS [1]	H0x08
Default Value	0	0	0	0	0	0	0	1	

Bits 7 to 0: SET_IBIAS[8:1]. The bias current DAC is controlled by a total of 9 bits. The SET_IBIAS[8:1] bits are used to set the bias current with even denominations from 0 to 510 bits. The LSB (SET_IBIAS[0]) is controlled by the BIASINC register and is used to set the odd denominations in the SET_IBIAS[8:0]. Any direct write to SET_IBIAS[8:1] resets the LSB.

Modulation Current Setting Register (SET_IMOD)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	SET_IMOD [8] (MSB)	SET_IMOD [7]	SET_IMOD [6]	SET_IMOD [5]	SET_IMOD [4]	SET_IMOD [3]	SET_IMOD [2]	SET_IMOD [1]	H0x09
Default Value	0	0	0	0	0	1	0	0	

Bits 7 to 0: SET_IMOD[8:1]. The modulation current DAC is controlled by a total of 9 bits. The SET_IMOD[8:1] bits are used to set the modulation current with even denominations from 0 to 510 bits. The LSB (SET_IMOD[0]) is controlled by the MODINC register and is used to set the odd denominations in the SET_IMOD[8:0]. Any direct write to SET_IMOD[8:1] resets the LSB.

Maximum Modulation Current Setting Register (IMODMAX)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	IMODMAX [7] (MSB)	IMODMAX [6]	IMODMAX [5]	IMODMAX [4]	IMODMAX [3]	IMODMAX [2]	IMODMAX [1]	IMODMAX [0] (LSB)	H0x0A
Default Value	0	0	1	0	0	0	0	0	

Bits 7 to 0: IMODMAX[7:0]. The IMODMAX register is an 8-bit register that can be used to limit the maximum modulation current. IMODMAX[7:0] is continuously compared to SET_IMOD[8:1]. Any attempt to modify SET_IMOD[8:1] above IMODMAX[7:0] is ignored and flags a warning at IMODERR.

Maximum Bias Current Setting Register (IBIASMAX)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	IBIASMAX [7] (MSB)	IBIASMAX [6]	IBIASMAX [5]	IBIASMAX [4]	IBIASMAX [3]	IBIASMAX [2]	IBIASMAX [1]	IBIASMAX [0] (LSB)	H0x0B
Default Value	0	0	1	0	0	0	0	0	

Bits 7 to 0: IBIASMAX[7:0]. The IBIASMAX register is an 8-bit register that can be used to limit the maximum bias current. IBIASMAX[7:0] is continuously compared to SET_IBIAS[8:1]. Any attempt to modify SET_IBIAS[8:1] above IBIASMAX[7:0] is ignored and flags a warning at IBIASERR.

Modulation Current Increment Setting Register (MODINC)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	SET_IMOD [0] (LSB)	X	X	MODINC [4] (MSB)	MODINC [3]	MODINC [2]	MODINC [1]	MODINC [0] (LSB)	H0x0C
Default Value	0	0	0	0	0	0	0	0	

Bit 7: SET_IMOD[0]. This is the LSB of the SET_IMOD[8:0] bits. This bit can only be updated by the use of MODINC[4:0].

Bits 4 to 0: MODINC[4:0]. This string of bits is used to increment or decrement the modulation current. When written to, the SET_IMOD[8:0] bits are updated. MODINC[4:0] are a two's complement string.

1Gbps to 11.3Gbps, SFP+ Laser Driver with Laser Impedance Mismatch Tolerance

Bias Current Increment Setting Register (BIASINC)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	SET_IBIAS [0] (LSB)	X	X	BIASINC [4] (MSB)	BIASINC [3]	BIASINC [2]	BIASINC [1]	BIASINC [0] (LSB)	H0x0D
Default Value	0	0	0	0	0	0	0	0	

Bit 7: SET_IBIAS[0]. This is the LSB of the SET_IBIAS[8:0] bits. This bit can only be updated by the use of BIASINC[4:0].

Bits 4 to 0: BIASINC[4:0]. This string of bits is used to increment or decrement the bias current. When written to, the SET_IBIAS[8:0] bits are updated. BIASINC[4:0] are a two's complement string.

Mode Control Register (MODECTRL)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	MODECTRL [7] (MSB)	MODECTRL [6]	MODECTRL [5]	MODECTRL [4]	MODECTRL [3]	MODECTRL [2]	MODECTRL [1]	MODECTRL [0] (LSB)	H0x0E
Default Value	0	0	0	0	0	0	0	0	

Bits 7 to 0: MODECTRL[7:0]. The MODECTRL register enables the user to switch between normal and setup modes. The setup mode is achieved by setting this register to H0x12. MODECTRL must be updated before each write operation. Exceptions are MODINC and BIASINC, which can be updated in normal mode.

Pulse-Width Control Register (SET_PWCTRL)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	X	X	X	SET_PWCTRL [3] (MSB)	SET_PWCTRL [2]	SET_PWCTRL [1]	SET_PWCTRL [0] (LSB)	H0x0F
Default Value	X	X	X	X	0	0	0	0	

Bits 3 to 0: SET_PWCTRL[3:0]. This is a 4-bit register used to control the eye crossing by adjusting the pulse width.

Deemphasis Control Register (SET_TXDE)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	X	SET_TXDE [5] (MSB)	SET_TXDE [4]	SET_TXDE [3]	SET_TXDE [2]	SET_TXDE [1]	SET_TXDE [0] (LSB)	H0x10
Default Value	X	X	0	0	0	0	0	1	

Bits 5 to 0: SET_TXDE[5:0]. This is a 6-bit register used to control the amount of deemphasis on the transmitter output. When calculating the total modulation current, the amount of deemphasis must be taken into account. The deemphasis is set as a percentage of modulation current.

Equalization Control Register (SET_TXEQ)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	X	X	X	X	SET_TXEQ [2]	SET_TXEQ [1]	X	H0x11
Default Value	X	X	X	X	X	0	0	X	

Bits 2 to 1: SET_TXEQ[2:1]. These 2 bits are used to control the amount of equalization on the transmitter input. See Table 1 for more information.

Design Procedure

Programming Bias Current

1) IBIASMAX[7:0] = Maximum_Bias_Current_Value
2) $SET\_IBIAS_i[8:1]$ = Initial_Bias_Current_Value

Note: The total bias current is calculated using the SET_IBIAS[8:0] DAC value. SET_IBIAS[8:1] are the bits that can be manually written. SET_IBIAS[0] can only be updated using the BIASINC register.

When implementing an APC loop it is recommended to use the BIASINC register, which guarantees the fastest bias current update.

3) $BIASINC_i[4:0]$ = New_Increment_Value
4) If ($SET\_IBIAS_i[8:1] \le$ IBIASMAX[7:0]), then ($SET\_IBIAS_i[8:0] = SET\_IBIAS_{i-1}[8:0] + BIASINC_i[4:0]$)
5) Else ($SET\_IBIAS_i[8:0] = SET\_IBIAS_{i-1}[8:0]$)

The total bias current can be calculated as follows:

6) $I_{BIAS} = [SET\_IBIAS_i[8:0] + 16] \times 200\mu A$

Programming Modulation Current

1) IMODMAX[7:0] = Maximum_Modulation_Current_Value
2) $SET\_IMOD_i[8:1]$ = Initial_Modulation_Current_Value x 1.06

Note: The total modulation laser current is calculated using the SET_IMOD[8:0] DAC value and the SET_TXDE register value. SET_IMOD[8:1] are the bits that can be manually written. SET_IMOD[0] can only be updated using the MODINC register.

When implementing modulation compensation, it is recommended to use the MODINC register, which guarantees the fastest modulation current update.

3) $MODINC_i[4:0]$ = New_Increment_Value
4) If ($SET\_IMOD_i[8:1] \le$ IMODMAX[7:0]), then ($SET\_IMOD_i[8:0] = SET\_IMOD_{i-1}[8:0] + MODINC_i[4:0]$)
5) Else ($SET\_IMOD_i[8:0] = SET\_IMOD_{i-1}[8:0]$)

The following equations give the modulation current (peak-to-peak) seen at the laser when driven differentially. R_{EXTD} is the differential load impedance of the laser plus any added series resistance.

6a) TXDE_MD[1:0] = 00, then

$$I_{MOD} = \begin{bmatrix} 0.3mA(SET\_IMOD[8:0]+16) \\ -0.15mA(SET\_IMOD[8:3]+2) \end{bmatrix} \times \frac{50\Omega}{50\Omega + R_{LD}}$$

6b) TXDE_MD[1:0] = 01, then

$$I_{MOD} = \begin{bmatrix} 0.3mA(SET\_IMOD[8:0]+16) \\ -0.15mA(SET\_IMOD[8:4]+1) \end{bmatrix} \times \frac{50\Omega}{50\Omega + R_{LD}}$$

6c) TXDE_MD[1:0] = 10, then set SET_TXDE[5:0] can be set to any value ≥ SET_IMOD[8:4] and

$$I_{MOD} = \begin{bmatrix} 0.3mA(SET\_IMOD[8:0]+16) \\ -0.15mA(SET\_TXDE[5:0]+1) \end{bmatrix} \times \frac{50\Omega}{50\Omega + R_{LD}}$$

When SET_TXDE[5:0] is increased, the deemphasis current increases and the overall peak-to-peak modulation current decreases. This effect saturates when SET_TXDE[5:0] = 0.2 x (SET_IMOD[8:0] + 16) - 1, and further increases to SET_TXDE[5:0] do not increase the deemphasis current.

6d) TXDE_MD[1:0] = 11, then

$$I_{MOD} = 0.9 \times \left[0.3mA(SET\_IMOD[8:0]+16)\right] \times \frac{50\Omega}{50\Omega + R_{LD}}$$

Note: When TXDE_MD[1:0] = 10 and the SET_TXDE register is set by the user, the minimum allowed deemphasis is 3% and the maximum is 10%. These limits are internally set by the MAX3946.

Programming Transmit Output Deemphasis

1) TXDE_MD[1:0] = Transmit_Deemphasis_Mode
2) SET_TXDE[5:0] = Transmit_Deemphasis_Value. If TXDE_MD[1:0] = 00, 01, or 11, the value of SET_TXDE is automatically set by the device and there is no need to enter data to SET_TXDE.

For Transmit_Deemphasis_Mode:

00 = deemphasis is fixed at 6% of the modulation amplitude (the device controls the SET_TXDE value), default setting

01 = deemphasis is fixed at 3% of the modulation amplitude (the device controls the SET_TXDE value)

10 = deemphasis is programmed by the SET_TXDE register setting

11 = deemphasis is at its maximum of approximately 9% (the device controls the SET_TXDE value)

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Programming Pulse-Width Control

The eye crossing at the Tx output can be adjusted using the SET_PWCTRL register. Table 5 shows these settings. The sign of the number specifies the direction of pulse-width distortion. The code of 1111 corresponds to a balanced state for differential output. The pulse-width distortion is bidirectional around the balanced state (see the *Typical Operating Characteristics* section).

Table 5. Eye-Crossing Settings for SET_PWCTRL

SET_PWCTRL[3:0]	PWD	SET_PWCTRL[3:0]	PWD
1000	-7	0111	8
1001	-6	0110	7
1010	-5	0101	6
1011	-4	0100	5
1100	-3	0011	4
1101	-2	0010	3
1110	-1	0001	2
1111	0	0000	1

Applications Information

Laser Safety and IEC 825

Using the MAX3946 laser driver alone does not ensure that a transmitter design is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Each user must determine the level of fault tolerance required by the application, recognizing that Maxim products are neither designed nor authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application in which the failure of a Maxim product could create a situation where personal injury or death could occur.

Table 6. Register Summary

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER/ TYPE	BIT NAME	DEFAULT VALUE	NOTES
Transmitter Control Register **Address = H0x05**	TXCTRL	R	RW	5	TXDE_MD[1]	0	MSB deemphasis mode
		R	RW	4	TXDE_MD[0]	0	LSB deemphasis mode
		R	RW	3	TXEQ_EN	0	Input equalization 0: disabled, 1: enabled
		R	RW	2	SOFTRES	0	Global digital reset
		R	RW	1	TX_POL	1	Tx polarity 0: inverse, 1: normal
		R	RW	0	TX_EN	1	Tx control 0: disabled, 1: enabled
Transmitter Status Register 1 **Address = H0x06**	TXSTAT1	R	R	7 (sticky)	FST[7]	X	TX_POR→TX_VCC low-limit violation
		R	R	6 (sticky)	FST[6]	X	BMON open/shorted to V_{CC}
		R	R	4 (sticky)	FST[4]	X	BMAX current exceeded or open/short to ground
		R	R	3 (sticky)	FST[3]	X	$V_{TOUT+/-}$ common-mode low-limit
		R	R	2 (sticky)	FST[2]	X	$V_{TOUT+/-}$ low-limit violation
		R	R	1 (sticky)	FST[1]	X	BIAS open or shorted to ground
		R	R	0 (sticky)	TX_FAULT	X	Copy of FAULT signal in case POR bits 6 to 1 reset to 0

Table 6. Register Summary (continued)

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER/ TYPE	BIT NAME	DEFAULT VALUE	NOTES
Transmitter Status Register 2 **Address = H0x07**	TXSTAT2	R	R	3 (sticky)	IMODERR	X	Warning increment result > IMODMAX
		R	R	2 (sticky)	IBIASERR	X	Warning increment result > IBIASMAX
		R	R	1 (sticky)	TXED	X	Tx edge detection
Bias Current Setting Register **Address = H0x08**	SET_IBIAS	R	RW	7	SET_IBIAS[8]	0	MSB bias DAC
		R	RW	6	SET_IBIAS[7]	0	
		R	RW	5	SET_IBIAS[6]	0	
		R	RW	4	SET_IBIAS[5]	0	
		R	RW	3	SET_IBIAS[4]	0	
		R	RW	2	SET_IBIAS[3]	0	
		R	RW	1	SET_IBIAS[2]	0	
		R	RW	0	SET_IBIAS[1]	1	
		Accessible through REG_ADDR = H0x0D		7	SET_IBIAS[0]	0	LSB bias DAC
Modulation Current Setting Register **Address = H0x09**	SET_IMOD	R	RW	7	SET_IMOD[8]	0	MSB modulation DAC
		R	RW	6	SET_IMOD[7]	0	
		R	RW	5	SET_IMOD[6]	0	
		R	RW	4	SET_IMOD[5]	0	
		R	RW	3	SET_IMOD[4]	0	
		R	RW	2	SET_IMOD[3]	1	
		R	RW	1	SET_IMOD[2]	0	
		R	RW	0	SET_IMOD[1]	0	
		Accessible through REG_ADDR = H0x0C		7	SET_IMOD[0]	0	LSB modulation DAC
Maximum Modulation Current Setting Register **Address = H0x0A**	IMODMAX	R	RW	7	IMODMAX[7]	0	MSB modulation limit
		R	RW	6	IMODMAX[6]	0	
		R	RW	5	IMODMAX[5]	1	
		R	RW	4	IMODMAX[4]	0	
		R	RW	3	IMODMAX[3]	0	
		R	RW	2	IMODMAX[2]	0	
		R	RW	1	IMODMAX[1]	0	
		R	RW	0	IMODMAX[0]	0	LSB modulation limit
Maximum Bias Current Setting Register **Address = H0x0B**	IBIASMAX	R	RW	7	IBIASMAX[7]	0	MSB bias limit
		R	RW	6	IBIASMAX[6]	0	
		R	RW	5	IBIASMAX[5]	1	
		R	RW	4	IBIASMAX[4]	0	
		R	RW	3	IBIASMAX[3]	0	
		R	RW	2	IBIASMAX[2]	0	
		R	RW	1	IBIASMAX[1]	0	
		R	RW	0	IBIASMAX[0]	0	LSB bias limit

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Table 6. Register Summary (continued)

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER/ TYPE	BIT NAME	DEFAULT VALUE	NOTES
Modulation Current Increment Setting Register **Address = H0x0C**	MODINC	R	R	7	SET_IMOD[0]	0	LSB of SET_IMOD DAC register address = H0x09
		RW	RW	4	MODINC[4]	0	MSB MOD DAC two's complement
		RW	RW	3	MODINC[3]	0	
		RW	RW	2	MODINC[2]	0	
		RW	RW	1	MODINC[1]	0	
		RW	RW	0	MODINC[0]	0	LSB MOD DAC two's complement
Bias Current Increment Setting Register **Address = H0x0D**	BIASINC	R	R	7	SET_IBIAS[0]	0	LSB of SET_IBIAS DAC register address = H0x08
		RW	RW	4	BIASINC[4]	0	MSB bias DAC two's complement
		RW	RW	3	BIASINC[3]	0	
		RW	RW	2	BIASINC[2]	0	
		RW	RW	1	BIASINC[1]	0	
		RW	RW	0	BIASINC[0]	0	LSB bias DAC two's complement
Mode Control Register **Address = H0x0E**	MODECTRL	RW	RW	7	MODECTRL[7]	0	MSB mode control
		RW	RW	6	MODECTRL[6]	0	
		RW	RW	5	MODECTRL[5]	0	
		RW	RW	4	MODECTRL[4]	0	
		RW	RW	3	MODECTRL[3]	0	
		RW	RW	2	MODECTRL[2]	0	
		RW	RW	1	MODECTRL[1]	0	
		RW	RW	0	MODECTRL[0]	0	LSB mode control
Pulse-Width Control Register **Address = H0x0F**	SET_ PWCTRL	R	RW	3	SET_PWCTRL[3]	0	MSB Tx pulse-width control
		R	RW	2	SET_PWCTRL[2]	0	
		R	RW	1	SET_PWCTRL[1]	0	
		R	RW	0	SET_PWCTRL[0]	0	LSB Tx pulse-width con-trol
Deemphasis Control Register **Address = H0x10**	SET_TXDE	R	RW	5	SET_TXDE[5]	0	MSB Tx deemphasis
		R	RW	4	SET_TXDE[4]	0	
		R	RW	3	SET_TXDE[3]	0	
		R	RW	2	SET_TXDE[2]	0	
		R	RW	1	SET_TXDE[1]	0	
		R	RW	0	SET_TXDE[0]	1	LSB Tx deemphasis
Equalization Control Register **Address = H0x11**	SET_TXEQ	R	RW	2	SET_TXEQ[2]	0	Tx equalization
		R	RW	1	SET_TXEQ[1]	0	

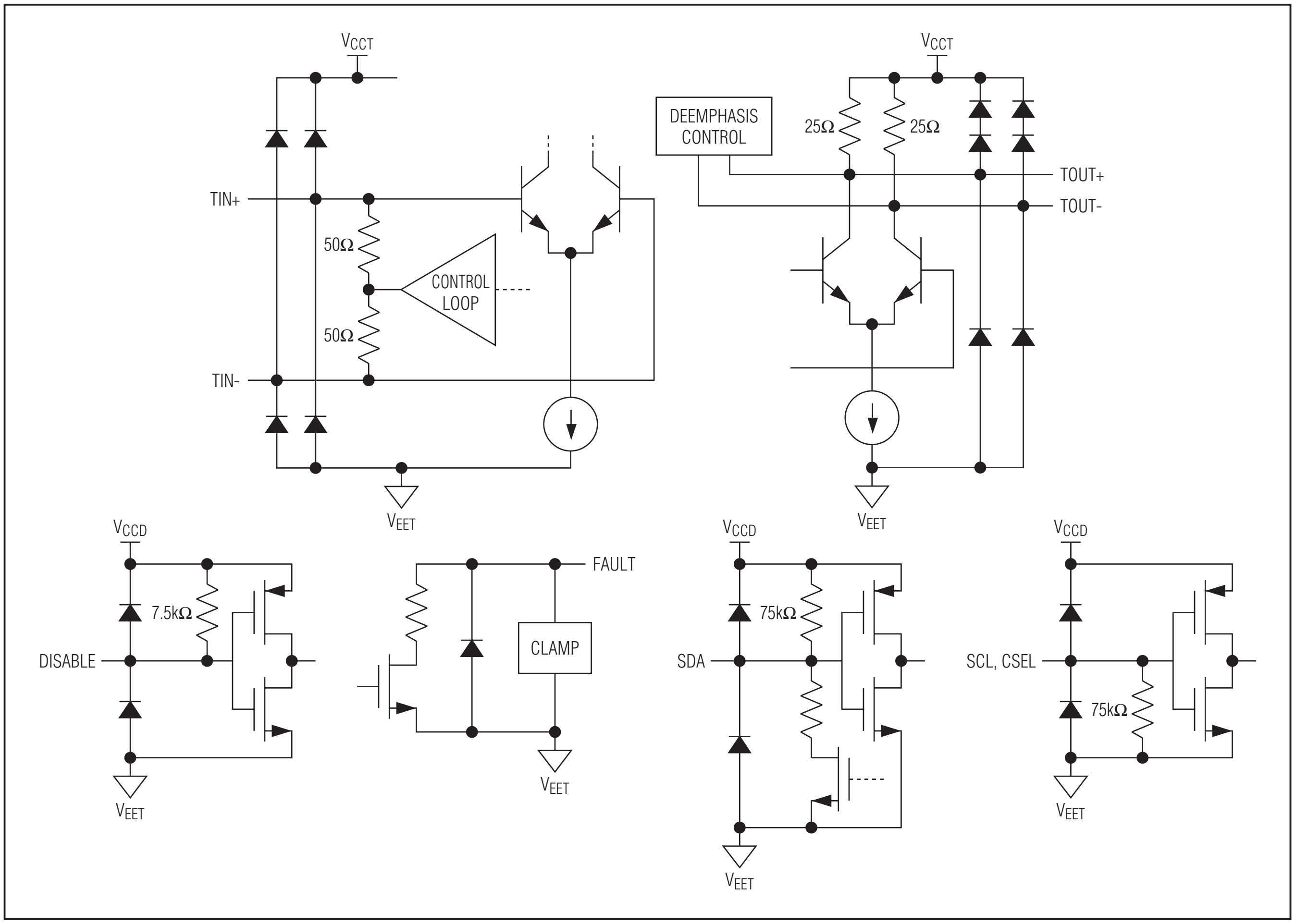


Figure 6. Simplified I/O Structures

Layout Considerations

The data inputs and outputs are the most critical paths for the device and great care should be taken to minimize discontinuities on these transmission lines between the connector and the IC. Here are some suggestions for maximizing the performance of the IC:

- The data inputs should be wired directly between the module connector and IC without stubs.
- The data transmission lines to the laser should be kept as short as possible and be designed for 50Ω differential or 25Ω single-ended characteristic impedance.
- An uninterrupted ground plane should be positioned beneath the high-speed I/Os.
- Ground path vias should be placed close to the IC and the input/output interfaces to allow a return current path to the IC and the laser.
- Maintain 100Ω differential transmission line impedance into the IC.
- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.

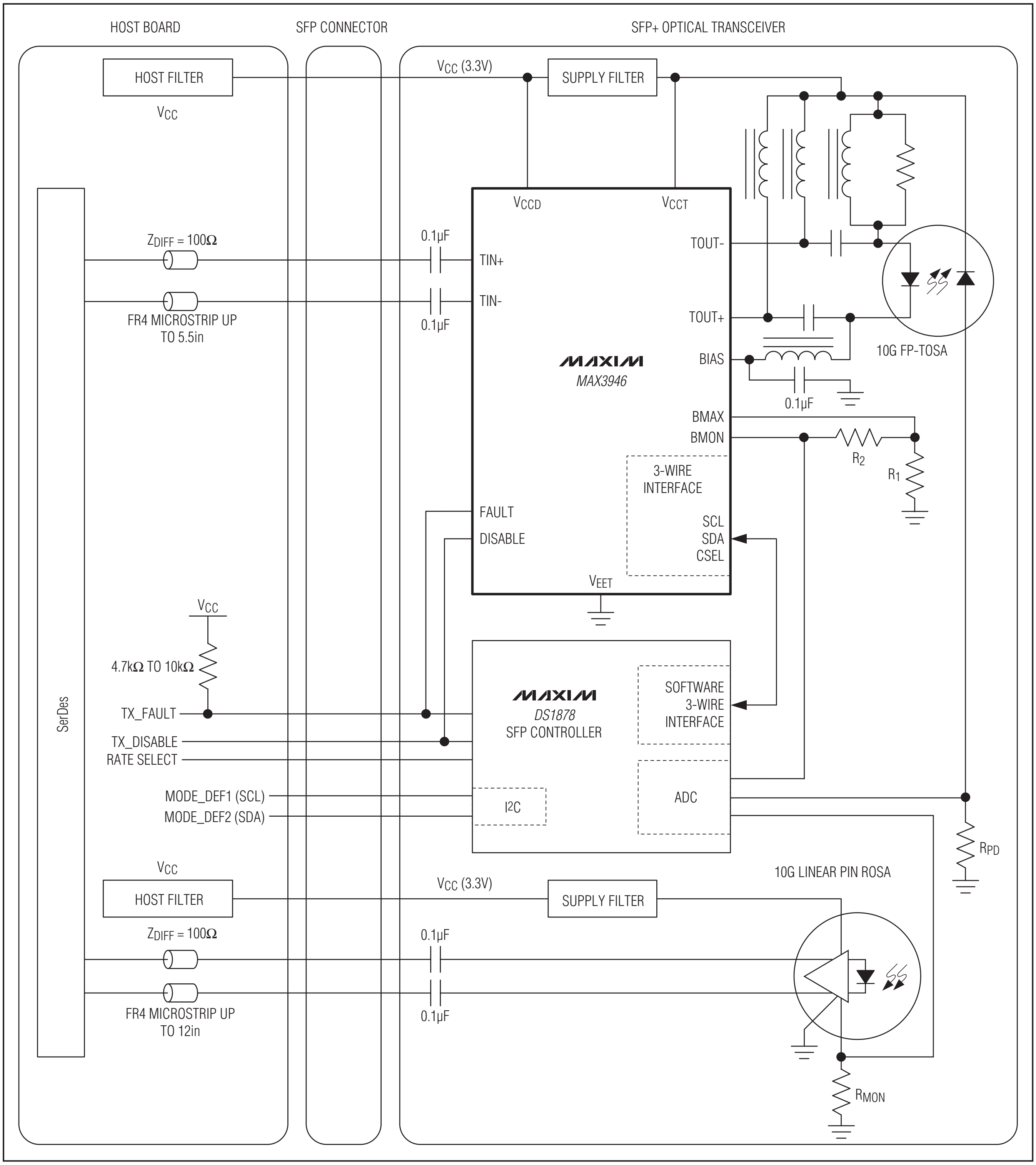
Refer to the schematic and board layers of the MAX3946 Evaluation Kit (MAX3946EVKIT) for more information.

Exposed-Pad Package and Thermal Considerations

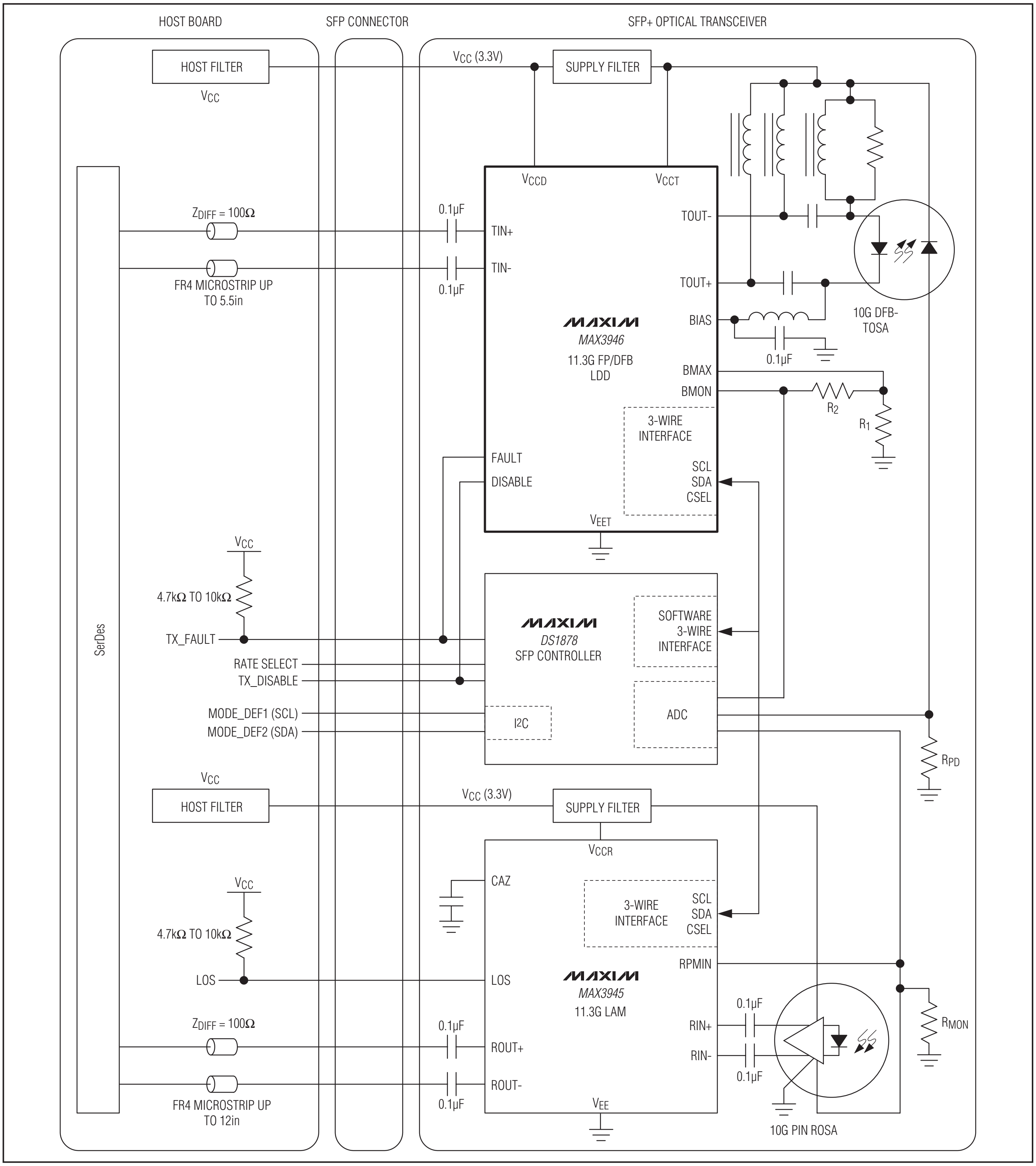
The exposed pad on the 24-pin TQFN provides a very low-thermal resistance path for heat removal from the IC. The pad is also electrical ground on the IC and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages* for additional information.

1Gbps to 11.3Gbps, SFP+ Laser Driver with Laser Impedance Mismatch Tolerance

Typical Application Circuit for 10GBASE-LRM



Typical Application Circuit for 10GBASE-LR



1Gbps to 11.3Gbps, SFP+ Laser Driver with Laser Impedance Mismatch Tolerance

Chip Information

PROCESS: SiGe BiPOLAR

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+3	**21-0139**	**90-0021**

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/10	Initial release	—
1	5/11	Changed the title from 1.0625Gbps to 1Gbps; changed the edge speed from 20ps to 22ps in the *General Description* and *Features*; added the *Package Thermal Characteristics* section; updated graphs 2, 10, 16, and 17 and replaced graphs 6 and 7 in the *Typical Operating Characteristics* section; updated the BIAS (requires a 0.1µF capacitor to V_{EET}) and CSEL (pulled down to V_{EET} rather than GND) pin descriptions in the *Pin Description* table; updated Figure 2 SCL and CSEL connections; changed the increment value range from -8 to +7 LSBs to -16 to +15 LSBs in the *Bias Current DAC* and *Modulation Current DAC* sections; changed the ground symbols to V_{EET} in Figure 4; updated the Transmitter Control Register (TXCTRL) bit 2 (SOFTRES) description; updated Figure 6, *Typical Application Circuit for 10GBASE-LRM*, and *Typical Application Circuit for 10GBASE-LR;* added the land pattern no. to the *Package Information* table	1, 2, 7, 8, 10, 11, 12, 14, 17, 25–28

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